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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,732	04/25/2001	Craig S. Sander	039153-0433 (C167596-CIP)	1672

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Joseph N. Ziebert
FOLEY & LARDNER
Firstar Center
777 East Wisconsin Avenue
Milwaukee, WI 53202-5367

EXAMINER	
NGUYEN, THANH T	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 11/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,732	SANDER ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *11/3/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, see pages 2-4, filed 11/3/04, with respect to claims 19-38 have been fully considered and are persuasive. The rejection of claims 19-38 has been withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 21-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Noble (U.S. Patent No. 5,976,930).

Referring to figures 2a-3, Noble teaches an integrated circuit including at least one transistor, the integrated circuit comprising:

A pair of local interconnects (200) spaced from each other; and

A gate of the transistor (170/161/162) disposed in the space between the local interconnects (200) and separated from of the local interconnects by an insulating liner (190),

wherein the space is less than or equal to the minimum lithographic feature (see figure 2a-3, col. 4, lines 26-25, col. 5, lines 55-67).

Regarding to claim 22, the pair of local interconnect (200) are space from each other by a minimum lithographic feature (see figure 2a-3, col. 4, lines 26-25, col. 5, lines 55-67).

Regarding to claim 23, the insulating liners (190) are each disposed on an interconnect wall adjacent the gate to separate each of the local interconnects from the gate (see figures 3).

Regarding to claim 24, a source and drain (135/136) are disposed by at least partially beneath the insulating liner (190).

Claims 19-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Gardner et al. (U.S. Patent No. 6,005,272).

Gardner et al. teaches an integrated circuit including at least one transistor, the integrated circuit comprising:

A pair of local interconnects (138a/138b) spaced from each other by a minimum lithographic feature and each being a minimum lithographic feature (see col. 5, lines 28-31); and

A gate of the transistor (134/144) disposed in the space between the local interconnects and separated from of the local interconnects by an insulating liner (150a/150b), wherein the space is less than or equal to the minimum lithographic feature, whereby the width of the transistor is not greater than three of the minimum lithographic feature (see figures 1a-1t, see col. 5, lines 28-31).

Regarding to claim 20, wherein the insulating liner (150a/150b) are each disposed on an interconnect wall adjacent the gate to separate each of the local interconnects from the gate (see figures 1P).

Regarding to claim 22, the pair of local interconnect are space from each other by a minimum lithographic feature (see figures 1k, see col. 5, lines 28-31).

Regarding to claim 23, the insulating liners (150a/150b/150c) are each disposed on an interconnect wall adjacent the gate to separate each of the local interconnects from the gate (see figures 1P).

Regarding to claim 24, a source and drain (138a/138b) are disposed by at least partially beneath the insulating liner (150a/150b/150c, see figure 1R).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bernhardt et al. (U.S. Patent No. 5,583,355) in view of ordinary skill person in the art.

Bernhardt et al. teaches an integrated circuit including at least one transistor, the integrated circuit comprising:

A pair of local interconnects (26a/26b) spaced from each other by a minimum lithographic feature and each being a minimum lithographic feature (see figure 1-3, col. 4, lines 7-15); and

A gate of the transistor (16/17) disposed in the space between the local interconnects and separated from of the local interconnects by an insulating liner (18), wherein the space is less than or equal to the minimum lithographic feature.

However, the reference does not specifically teach the width of the transistor is not greater than three of the minimum lithographic feature. Since Bernhardt et al. teaches the dimension of the transistor is not greater than two microns (see figure 1-3, col. 4, lines 7-15) it would be obvious that the width of the transistor in the range of less than two microns, for example, the transistor is 1 micron if the pair of local interconnect are 0.8 micron and the gate is 0.2 micron which is less than 3 minimum lithographic feature.

Therefore, it would have been obvious to an ordinary skill in the requisite art at the time of the invention was made would form a transistor wherein the width is not greater than three minimum lithographic feature because forming a transistor wherein the width is not greater than three minimum lithographic feature would provide more high density on the chip.

Regarding to claim 20, wherein the insulating liner (18) are each disposed on an interconnect wall adjacent the gate (16/17) to separate each of the local interconnects from the gate (see figures 1-3).

Regarding to claim 23, wherein the insulating liner (42) are each disposed on an interconnect wall adjacent the gate to separate each of the local interconnects from the gate (see figures 2g-2i).

Regarding to claim 24, the source and drain (21/22) are disposed by at least partially beneath the insulating liners (18, see figure 1).

Claims 25-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (U.S. Patent No. 5,940,710) in view of Liaw et al. (U.S. Patent No. 5,955,768).

Referring to figures 2a-2e, Chung et al. teaches an integrated circuit including at least a pair of local interconnects with one interconnect on each side of gate transistor, the integrated circuit being manufactured by a method comprising the steps of:

Forming on a semiconductor substrate (1) a thick insulating layer (6);

Forming at least a pair of space apart openings (30) in the insulating layer adjacent the semiconductor substrate (1);

Forming a source (14) in one of the openings (30) and the drain (14) in one of the openings;

Filling each of the openings with a conductive material (8) to form the local interconnects (8), the local interconnect being electrically couple to the source and drain (14);

Removing a portion of the insulating layer (6) to form a gate opening between the local interconnects (8);

Forming a gate dielectric (4) on the semiconductor substrate (1) in the gate opening; and

Forming the gate (5) on the gate dielectric layer.

With regard to claims 25-26, 28-31, the terms "forming", "filling", "removing", "etch selectivity relative to" is method recitations in a device claimed, and they are non-limiting, because only the final product is relevant, not the method of making. A product by process claim is directed to the product per se, no matter how actually made. See also MPEP 2113.

Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Regarding to claim 27, see figure 2d.

Regarding claim 32, see figure 2e.

Regarding to claim 33, see figure 2e, col. 6, and lines 10-11.

Regarding to claims 37-38, the term "etching stop layer is formed on semiconductor substrate before forming the thick insulating layer" and "the etching selectivity" is method recitations in a device claimed, and they are non-limiting, because only the final product is relevant, not the method of making. A product by process claim is directed to the product per se, no matter how actually made. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Chung et al. teaches all of the limitations as described in the claimed invention above. However, Chung et al. does not teach or suggested an etching stop layer, and forming barrier layer Titanium nitride before forming conductive material tungsten.

Liaw et al. teaches forming an etching stop layer (40, silicon nitride) before forming the thick insulating layer (ILD), forming a barrier layer titanium nitride (42) in the opening (W4/W5) and forming a conductive material tungsten (PL2/PL3).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time the invention was made would form an etching stop layer (silicon nitride) before forming the thick insulating layer, forming a barrier layer titanium nitride in the opening and forming a conductive material tungsten in process Chung et al. as taught by Liaw et al. because

the process would prevent the chemical reaction between the conductive layer and the substrate by diffusion.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN